1.2 Analog and Mixed-Signal Innovation: The Process-Circuit-System-Application Interaction

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INTRODUCTION

At last year's ISSCC we heard intriguing and informative plenary talks by T.C. Chen of IBM's T.J. Watson Labs, and by Hermann Eul of Infineon Technologies. Dr. Chen addressed the claims of experts that Moore's Law is dead, and reviewed the challenges currently posed for deep-submicron CMOS, and the developments that are sure to keep the state-of-the-art moving to even more "astonishing capabilities." Dr. Eul discussed the incredible consumer pull that is challenging process developers, chip designers, and system architects, to pack ever-more features and functions into cellular handsets, but without consuming more power.

Those presentations highlighted the need for continuous innovation to ensure the future health of the electronics industry. Consequently, innovation in analog and mixed-signal electronics has become increasingly important to the continued growth of the semiconductor industry. Technologists working in the analog and mixed-signal arena certainly share with their digital counterparts the overarching goal of reducing power and cost-per-function in each IC generation. But they must also operate under physical constraints that, until recently, have been secondary in the digital world. By way of contrast, from the advent of the first analog IC, analog designers have exploited the potential of the process technology to develop circuits that minimize the impact of variation in process parameters on product performance. While process scaling has enabled the development of a wide variety of products, from cell phones to advanced medical imaging systems, the success of these products depends in large measure on their ease-of-use and seamless connection to wireless and wired networks. Analog and mixed-signal subsystems, including display drivers, WLAN, and cellular radios, support these critical interfaces. The downward scaling of supply voltage in deep-submicron CMOS, now at 1volt, may limit dynamic range, forcing some analog functions to be implemented on other processes, but it has also enabled new circuit architectures that gain back dynamic range.

Moore's Law & More

The International Technology Roadmap for Semiconductors (ITRS) represents Moore's law at work, along with the diversified analog/mixed-signal functions required for system interface, in a compelling chart (Figure 1.2.1). The left axis illustrates Moore's Law, with scaling benefiting various purely digital devices such as CPUs, memory, and logic, for information processing. Continued process scaling has allowed chip designers to combine pretty much any digital function they need into an SoC, and has, without question, fueled the growth of the semiconductor industry. On the top axis of Fig. 1.2.1, we see the various functions and technologies required to interface, or interact with, the "real world" of people and the environment. These interface functions often limit a system's performance, and subsequent usability, and continued improvement is critical for driving industry growth. The diagonal vector represents the combination of process scaling and functionality that is required for complex, higher-value systems.

Scaling is without question a good thing, and definitely allows the integration of an increasing number of digital functions. However, the components and technologies necessary to interact with the real world do not necessarily scale. In fact, there is a great diversity in process and manufacturing technologies required to build passives, RF, high-voltage power circuits, and a host of sensor actuator devices. For decades, analog and mixed-signal designers had to innovate to push past the limitations that the variability of silicon posed, in order to achieve improvements in performance. Now, as the state-of-the-art for digital CMOS has reached 65nm, and is still dropping, process variability has now become a major issue, and poses challenges to digital designers similar to those that analog designers have dealt with for years.

Analog & Mixed-Signal Real-World Interface

Many different types of applications exist for electronic systems today, and all of them require a real-world interface into the system, out of the system, or both (Figure 1.2.2). The end application determines two things: the kind of interface that is required, and the level of performance necessary to meet system needs. While the digital portion of each system may be impolitely called "variations on a theme", the wide variety of real-world interfaces requires many different types of innovative processes and design techniques to meet economic and performance goals. From a system perspective, however, these two worlds, of analog and of digital, overlap and cannot be treated separately. Instead, the industry must take an interdisciplinary approach to innovating in all areas of the design process: the end application; system architecture; circuit design; semiconductor process; and real-world interfaces. In Fig. 1.2.2, the inner circle represents the interaction and interdependencies between process, design, system, and application.

In recognition of this interdependency, ISSCC has invited 5 presentations from the December 2006 International Electron-Devices Meeting (IEDM) to be repeated for ISSCC attendees, for the first time at ISSCC, bringing these two worlds of process and circuit design together.

The Innovation Cycle

Today, applications are the dominant driver of the electronics industry, and require performance, flexibility, and ease-of of-use at low cost and low power (Figure 1.2.3). Increased integration and lower cost will ensure that this cycle will continue. But, meeting this challenge requires intense interaction between circuit design, process development, and system engineering, to satisfy the demands of applications. In turn, development of innovative IC technologies enables new applications.

A Brief History of the Semiconductor Industry

Process limitations are nothing new for designers of analog and mixed-signal devices. Moving from circuits built from discrete components to designing in the first planar bipolar processes posed challenges back in the 1960s and 1970s. The available suite of components was limited, forcing circuit designers to collaborate with process developers to expand the repertoire of usable components [1] [2]. Just as today, system requirements were the key drivers, and integration and miniaturization were the main goals.

It's worth taking a look at the history of semiconductor-technology development, and its key drivers (Figure 1.2.4). The invention of the Planar process, which made the manufacture of integrated circuits on silicon practical, by Jean Hoerni and his colleagues at Fairchild in the late 1950s, set the stage for the development of the first IC op amp in 1964. As system requirements have changed and become more demanding, far more complex processes have been developed. Today, processes ranging from SiGe BiCMOS to 100V DMOS to 65nm CMOS are required to optimally support myriad systems.

Some of the applications, markets, and end-equipment products became the drivers for the semiconductor industry. If we were to try and find a single point in history that represented the beginning for personal consumer electronics, the fastest-growing semiconductor market, it could well be the introduction of the Sony

Walkman™. It was personal, affordable, and portable. It's easy to trace a line from the Walkman™ to portable CD players, today's MP3 players, and cell phones. A key enabler was the development of the microprocessor, which led to systems designed to economically process data at high speed. Continued integration and falling microprocessor costs drove the development of data converters, initially to play back pre-recorded media, and then also to record via audio codecs (coder-decoder). Cost and power consumption continued to fall, and data- conversion and signal-processing functions became ubiquitous in consumer electronics, as well as in the domain of instrumentation and industrial-process control.

Developments in MOS devices led to RCA's invention of COS/MOS, which stands for **CO**mplementary **S**ymmetry **M**etal **O**xide **S**emiconductor [3]. PMOS was developed for watches, but NMOS was developed for complex digital circuits that required significantly more speed, and was used extensively by semiconductor companies. CMOS evolved from COS/MOS in parallel with these other developments, however, and not in a linear fashion. Its complementary structures were useful in data-converter design. In fact, one of the greatest innovations in the semiconductor industry was the development of complementary structures that allow simpler circuit designs that consume less power.

But what could be done if system requirements could best be met with an MOS process? Here again, discovering and exploiting inherent characteristics of the process allowed data converters to be built in MOS as well as in bipolar processes. MOS does not favor construction of low-TC resistors, a desirable component for data converters and many other circuits. However, MOS has high-quality capacitors and, more importantly, they offer good ratio matching that results in robust circuits. A technique using charge redistribution with switched capacitors [4] [5] [6] allowed designers to replace resistors with capacitors, and, more importantly, allowed the scaling that set the stage for analog VLSI. Starting at 5 microns, switched-capacitor circuits have successfully scaled down to 65nm with no end in sight!

Variability and the Evolution of the Bandgap Voltage Reference

In the 1960s and 1970s, systems needed precision components such as op amps with 100mV offset voltage and 10 bit ADCs, but the process capabilities of the time did not readily support this level of precision. As a consequence, a number of circuit techniques were developed to overcome process limitations, and achieve high performance from a low-accuracy process. The ten-year evolution of the bandgap voltage reference, starting with Hilbiber's impractical differential reference [7], to Widlar's two-terminal reference [8] [9], to Brokaw's three-terminal bandgap reference [10], is a good example (Figure 1.2.5a). Data converters were one of the key drivers for a stable and accurate voltage reference. For a converter to produce an accurate output, it has to have an accurate voltage reference with a low temperature coefficient. The other key driver was the need for good voltage regulators for use in myriad power applications, including power supplies and automotive systems [4].

Discrete reference circuits were based on zener diodes. They were accurate and stable, but required support components and a relatively high supply voltage, usually over 6 volts. This became a problem as systems were increasingly moving to 5 volt supplies for logic circuits. The curves in Figure 1.2.5b, show expected variation in resistor values, ΔV_{BE}, and a bandgap-reference output voltage. While the distribution of resistor values is ±20 percent, the bandgap reference takes advantage of the inherent tight matching of resistor ratios and the logarithmic relationship of V_{BE} to collector current to achieve an output voltage of ±5%, and a temperature coefficient 30ppm/°C without any trimming, thus compensating for process variability.

The bandgap reference enabled new circuit techniques, such as PTAT (Proportional To Absolute Temperature), operation which maintains constant transconductance in a bipolar transistor over temperature. It also spawned a great many voltage references and voltage regulators from many vendors for many different applications. Today, it's hard to find an analog or mixed-signal chip of any sort that doesn't contain one or more circuits based on a bandgap voltage reference.

Trim and the First Data Converters

It was important to find other techniques to achieve precision and accuracy that were less sensitive to process variations, and could meet analog-to-digital system specifications. The system needs of complete functionality and performance could not be met without some form of intervention. A number of techniques have been developed to trim out errors to improve yields and meet the target the system requirements, thereby controlling or counteracting process variability. A partial list of technology includes: laser-trimmed thin film [11] [12]; resistor matching or shuffling [13]; link blowing [14]; zener zapping [15]; dynamic element matching [16], and current matching/cancellation [2].

Complementary Processes Enable New Circuits

NMOS was popular for digital ICs, but its high power consumption presented a major limitation. And while bipolar had PNP transistors, lateral PNPs were typically limited to a 5MHz f_T. COS/MOS or CMOS structures featured complementarity that enabled circuit designs with much lower power consumption. Innovations in circuit architecture, such as the pipeline ADC [17], and improvements in CMOS processes, have enabled dramatic improvements in the performance of data converters. The figure-of-merit (FOM) for ADCs (Figure 1.2.6a), measured in joules per conversion step, has improved 10,000X since the early 1980s!

Complementary structures also played a major role in analog IC development. CB, or complementary bipolar, processes, offered a good vertical PNP and enabled faster linear circuits without increasing power consumption. In addition to taking advantage of the original planar process, the industry has also improved semiconductor processes for analog and mixed-signal circuits. Figure 1.2.6b chronicles nearly three decades of op amp performance, and shows improvement in bandwidth versus current. While bandwidth has increased by 1000X for the same amount of supply current, cost per MHz has dropped also by 1000X. In the late 70s, BiFET op amps incorporated a FET input structure that helped reduce power, while improving speed. The late 80s saw the development of the junction-isolated complementary bipolar process with an order of magnitude speed improvement, and, in the 90s, the silicon-on-isolator complementary bipolar process which enabled nearly two orders of magnitude improvement.

Despite the tremendous success of the op amp, other gain blocks were developed for instrumentation and oscilloscopes applications. Examples include "current-mode" amplifiers, and translinear circuits [18]. At a time when op amps were struggling to move past 1MHz, such ICs were achieving bandwidths of 500MHz.

Nanometer Scaling: New Possibilities

A fundamental trade-off between speed (f_T) and breakdown voltage - the Johnson limit - in semiconductors is shown in Fig. 1.2.7. It compares N-type devices because they are faster than P-type devices, given that electrons have greater mobility than holes. The left axis indicates f_Ts in GHz and illustrates the dramatic speed improvements in NMOS for each geometry shrink, starting with 0.5-micron. (The equivalent f_T for the NMOS devices is derived by extrapolating y21/y11 to 0dB at –20dB/decade). Smaller geometries were pursued to put more transistors on a given die, while the accompanying speed improvement allowed much greater digital bandwidth. To minimize power, however, lower supply voltages are used, which significantly reduces

dynamic range. In contrast, the bipolar curve indicates three times the speed of NMOS at 3 volts, allowing sufficient dynamic range for most real-world interface devices. The ten-fold increase in f_T of 65nm NMOS, to about 170GHz, compared to 18GHz at 0.5mm, opens up new opportunities for integrating millimeter-wave circuits. In fact, several papers at this Conference will report results of CMOS circuit operation at 100GHz or higher.

ADC Calibration

Various auto-calibration techniques have been employed to achieve accuracy in high-resolution converters. Such techniques usually require 2^n passes (where n is the number of bits) for the cycle to converge. The time consumed increases with increasing resolution. Converter calibration can be performed using multiple converter blocks, and a new and innovative algorithm that is deterministic and converges very quickly [19], as shown in Fig. 1.2.8. This approach exploits the scaling of sub-micron CMOS VLSI. Splitting the A-to-D into two halves reduces the silicon requirements. The plot to the lower right of Fig. 1.2. 9 shows actual measured INL (integral non-linearity), before and after calibration. The dotted line indicates well over 20 LSBs of error, and the solid line shows that calibration has reduced the error by 10X.

A very different approach is to eliminate, or minimize the need for, any precision components. The first examples were integrating "dual-slope" converters. Over-sampling, or delta-sigma conversion, eliminates precision components, allows direct trade-off between speed and resolution, and is easily integrated in complex digital chips. The delta-sigma architecture has proven extremely versatile, and is used in virtually every cell phone today [20].

If we step back, and look at analog-to-digital converter performance, what had been only incremental improvement until the late 90s has accelerated in the 21st century. The performance of pipeline converters, and of other types of ADCs continued to improve with each process shrink. Portable- system requirements are driving the need for better and faster converters. Chief among these applications are communication systems and medical imaging equipment. Besides better performance, system designers also wanted lower cost and lower power. Clearly, process shrinks have greatly benefited converter performance, but this improvement is also due to innovative use of new architectures, such as pipeline and delta-sigma.

Typical 2007 Cell-Phone Users Want it all: Challenges & Solutions

While the "wireless revolution" involves a number of different wireless products, one of the great drivers for semiconductor content is the cellular handset. Strategy Analytics projects 1 billion units for 2006 and nearly 1.2 billion for 2007. According to WSTS, total semiconductor revenues worldwide were $240 billion in 2005, with forecasts of $247 billion in 2006, $268 billion in 2007, and $300 billion in 2008. Gartner forecasts cell-phone semiconductor content to reach $60 billion by 2008. The cell-phone market is clearly driving every phase of the electronic design chain.

Current-generation cell phones are truly complex systems. A high-end model incorporates a digital camera, CD-quality audio playback, gaming, text messaging, and multi-band multi-mode radio transceivers, all with two- to-three-week standby time [Figure 1.2.10]. The demand for these features is driving the need for more and better analog interfaces. In addition, implementing all these features will require: a 100 to 500 MIPS programmable processor(s); a 2 to 6 GOPS hardware DSP; and multiple 16-bit ADCs DACs.

Since consumers are willing to pay for all these cell-phone features, handset designers are doing whatever is necessary to satisfy demand. The greatest challenge is to minimize interference and keep power usage down, preferably under 2 watts. The most significant problem is too many radios. For the basic voice call function a typical phone will process 2.5G and/or 3G [21], or 9 bands from 0.9 to 2.3GHz. In addition, consumers are coming to expect an FM radio at 100MHz for listening to local radio broadcasts; DAB/Satellite radio at 2.2GHZ; GPS at 1.5GHz [22]; as well as mobile TV. In addition, personal connectivity necessitates the inclusion of Bluetooth at 2.4GHz [23], and WiFi, also at 2.4GHz. Also in development, and coming soon, are WiBree, UWB, WiMAX, NFC, and RFID, all of which operate in multiple bands. If that's not a difficult enough design challenge, consider the unintentional RF radiation from the DSP, the main processor, and the I/O, with high-speed clocks. Although no single handset is likely to include all these radios, most will contain some significant combination. The design challenge will be to deal with interference, [24] [25], while keeping down both power and cost and size [26].

Micro-Machined Sensors for Portables and Cell Phones

Micro-machined IC technology enables new features such as phased-array microphones for higher quality audio. A 3-axis accelerometer (Figure 1.2.11) can be used to sense motion to control a cell phone, or to sense impact and trigger protection for sensitive components such as disc drives.

Classic Heterodyne versus Direct-Conversion Receivers: Challenge of Cost Reduction

Figure 1.2.12 shows the classic heterodyne receiver which has been used successfully for a long time. This radio exploits analog pre-processing, (filtering, amplification, frequency conversion) to realize a robust receiver. This complexity, however, makes this receiver too expensive for today's systems. The bottom block diagram illustrates a direct-conversion architecture, whereby the LNA output is immediately mixed, filtered, and fed into the ADC and digital-filter block. The IF section is removed and system complexity is reduced, which lowers cost [27]. The tradeoff is that error-correction and calibration are required to compensate for LO (local oscillator) leakage that shows up as a DC offset and requires that the ADCs must have higher performance.

The Rise and Fall of the Inductor

While process scaling, new architectures, and advanced circuit techniques have facilitated integration for some time, the physics of the real world eventually limits, or even stops, progress. Systems frequently require some components that simply don't scale or can't be integrated into silicon. Inductors are a case in point. The use of inductors in radios dates back to Marconi, as illustrated in Fig. 1.2.13. The lower curve shows the number of active devices used in each radio over the same period, and notes new inventions, such as the vacuum tube, the transistor, and the integrated circuit.

From a chip-design and system perspective, inductors pose a significant barrier to integration and miniaturization - they take up space. Beginning with the "wireless revolution" in the 80s, transistors have replaced inductors wherever possible. But the use of inductors will not go to zero, because of a simple factor: inductor-based oscillator circuits require less power than those based on transistors. That's because the phase noise of an oscillator varies as the inverse square of the inductor's Q [28], and furthermore, a ring oscillator may draw 400X more current than a simple LC oscillator for the same phase noise [29] [30]. For this reason, inductor usage is not going to zero. This has led designers to stack inductors on top of active components to save die area.

Challenges for ADC Sample Rate & Dynamic Range

The A/D converter continues to be an area of focus for reducing radio complexity. In light of the aforementioned improvements in converter performance, it would seem logical to move the converter closer to the signal source. and do everything, or almost everything, digitally. The challenge is to do so but not at the cost of increased power consumption. Figure 1.2.14a shows SNR (signal-to-noise ratio) in bits of resolution versus sample rate, and

depicts what is believed to be the physical limitations of converter design. While it indicates aperture jitter and the Heisenberg uncertainty factor, the key points are where the performance requirements fall for known applications. This point at 13 bits and 125MS/s [31] indicates the ADC performance required for a GSM base-station super-heterodyne receiver. The point at 15 bits and 1GS/s represents the performance required for direct RF sampling in a GSM base station. That means placing the converter right after the LNA. According to Walden's prediction [32] on converter-performance advances, it will be the year 2038 before we reach that point. But there is another way to solve the problem! By using analog pre-processing, system power can be reduced and a slower lower-resolution converter can be used in base stations. GSM cell phones place less-stringent demands on their receivers, and direct RF sampling has been demonstrated [33]. The demand for lower power continues to motivate the development of high-sample-rate ADCs that achieve figures of merit of 1pJ or less, as shown in Fig. 1.214b [34] [35] [36].

Conclusion

The creative combination of process, design, and system architecture, results in robust solutions for demanding applications, and will prove to be even more crucial in the future. Such solutions will be essential in meeting the challenges posed by the physical realities of deep-submicron design, in achieving gigahertz speeds, minimizing power consumption, and integrating multiple functions in smaller packages. Variability in semiconductor processes has been successfully handled for decades, but end-user applications, such as the cell phone, are placing increasing demands on high-performance analog, and will exceed the capabilities of current processes. This may necessitate pre-processing of signals in the analog domain, or it may be more effective to digitize the signal closer to the source, and rely on the flexibility of digital signal processing. More importantly, the industry must take an interdisciplinary approach to solving problems and meeting target system specifications, including design, process development, scaling, system architecture, and overall integration, to reduce cost. We must study the application requirements, develop appropriate system architectures, develop innovative circuit designs, and constantly work with process developers. Taking a holistic approach is the way forward to meet this challenge!

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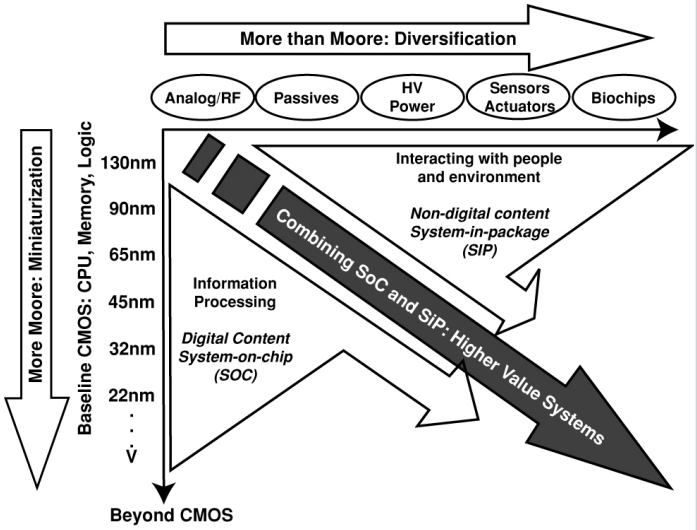


Figure 1.2.1: Moore's law and more.

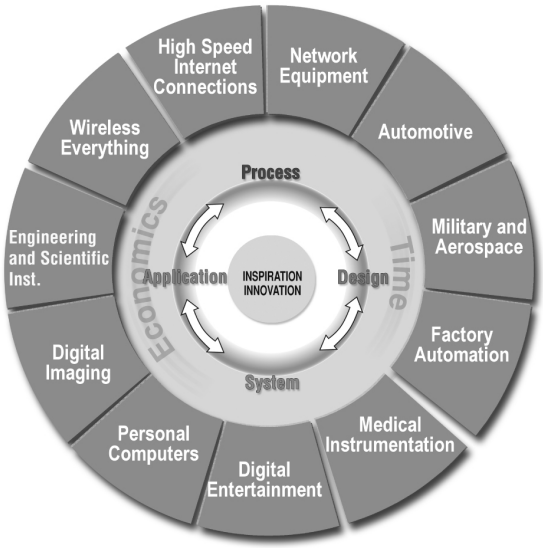
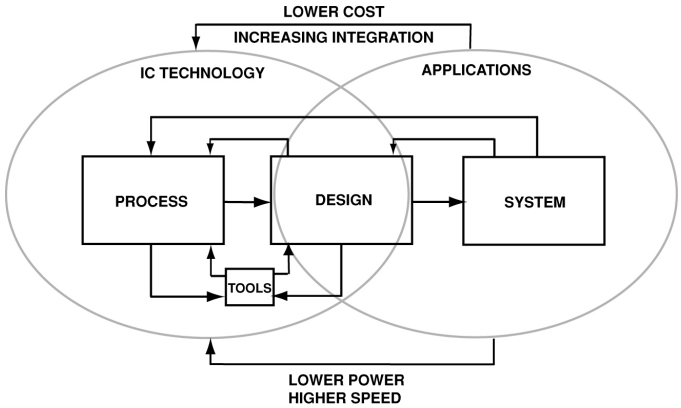


Figure 1.2.2: Analog and mixed-signal "real-world interface".



The Innovation Cycle
Applications Drive IC Technology: ICs Enable New Applications

Figure 1.2.3: The innovation cycle.

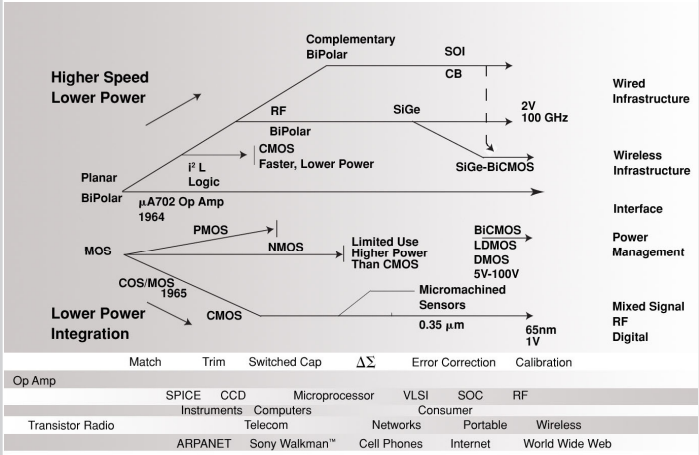
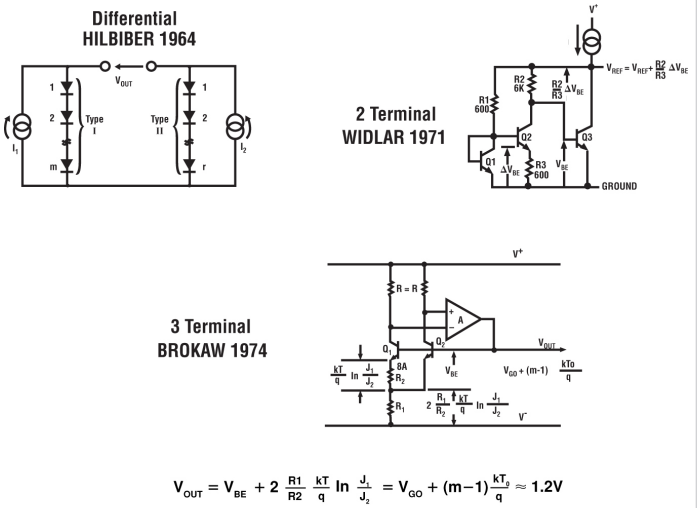
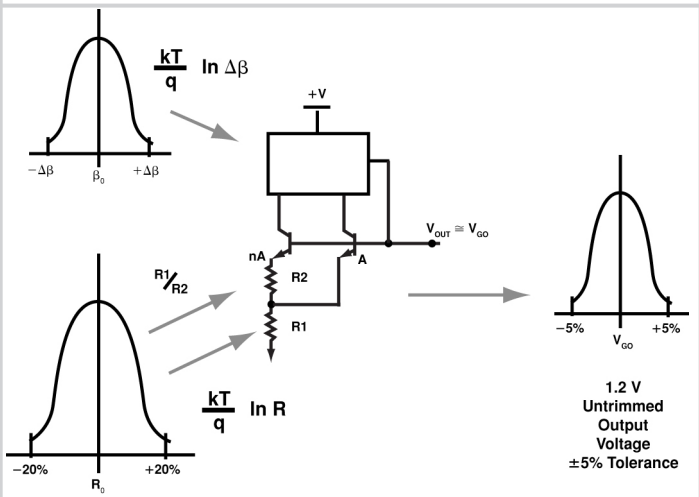


Figure 1.2.4: A brief history of the semiconductor industry.



$$V_{OUT} = V_{BE} + 2\frac{R1}{R2}\frac{kT}{q}\ln\frac{J_1}{J_2} = V_{GO} + (m-1)\frac{kT_0}{q} \approx 1.2V$$

Figure 1.2.5a: Variability and evolution of the bandgap voltage reference.



"Silicon knows how big a volt is." APB. Oct. 2006

Figure 1.2.5b: Variability and evolution of the bandgap voltage reference.

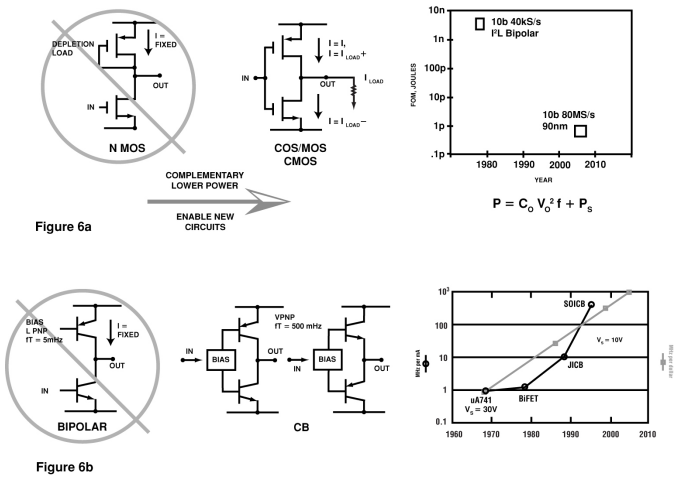


Figure 1.2.6: Complementary process enables new lower power circuits.

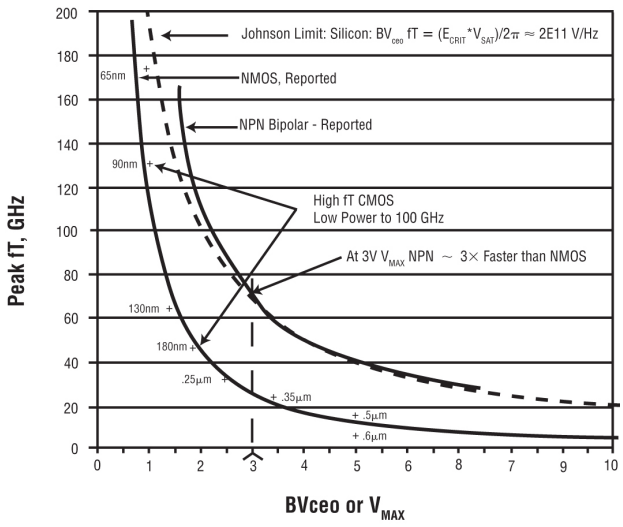


Figure 1.2.7: Nanometer scaling enables multi GHz circuits.

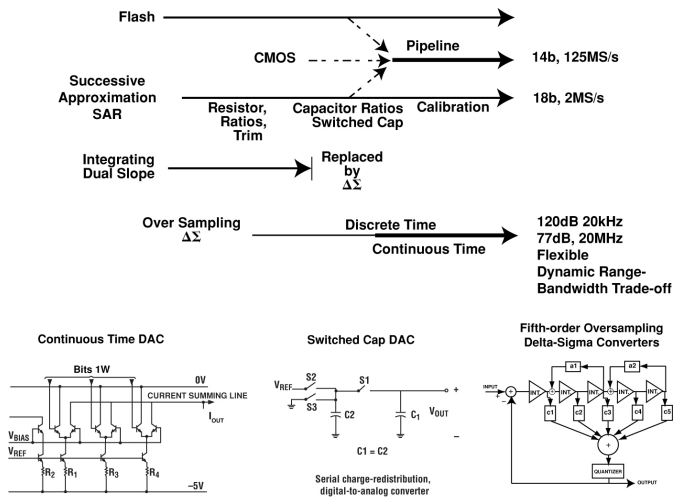


Figure 1.2.8: Evolution of ADCs.

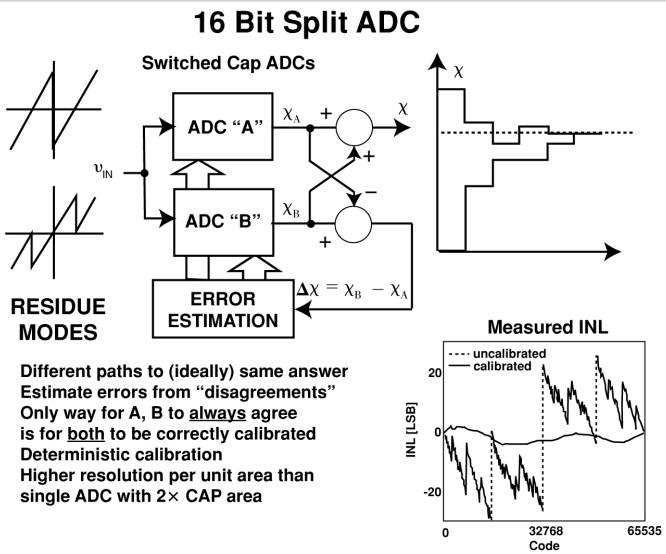


Figure 1.2.9: ADC calibration.

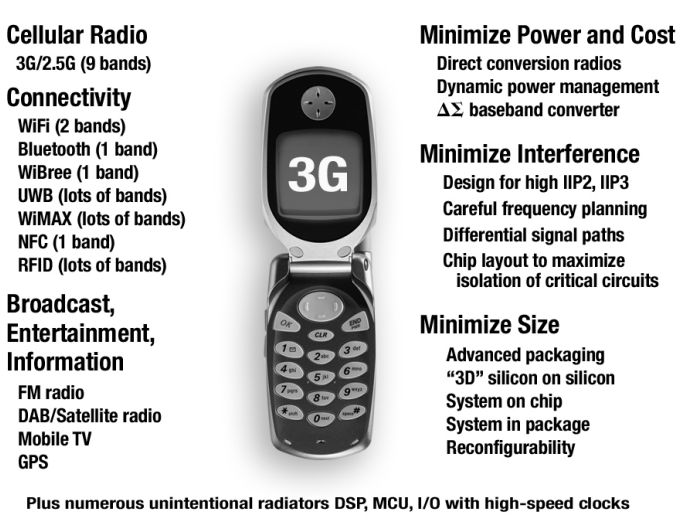


Figure 1.2.10: Typical 2007 cell phone: Challenges and solutions.

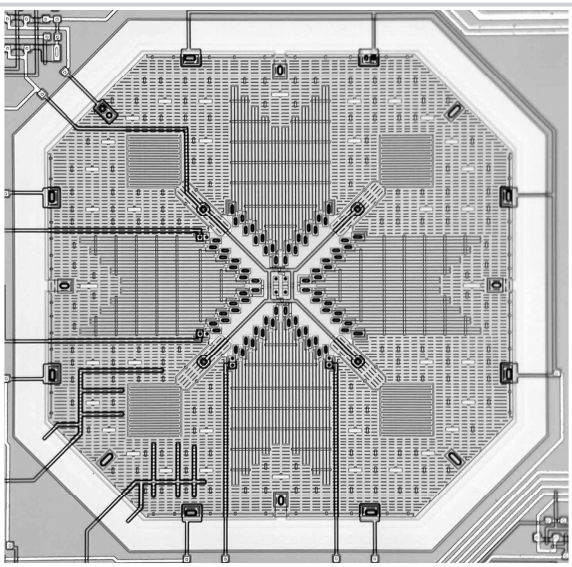


Figure 1.2.11: Three-axis accelerometer, sensor with pre-processing.

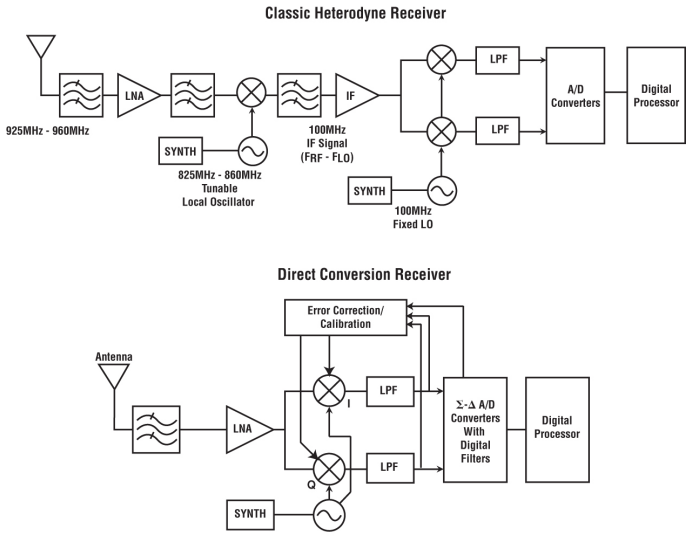


Figure 1.2.12: Classic heterodyne versus direct conversoin receiver.

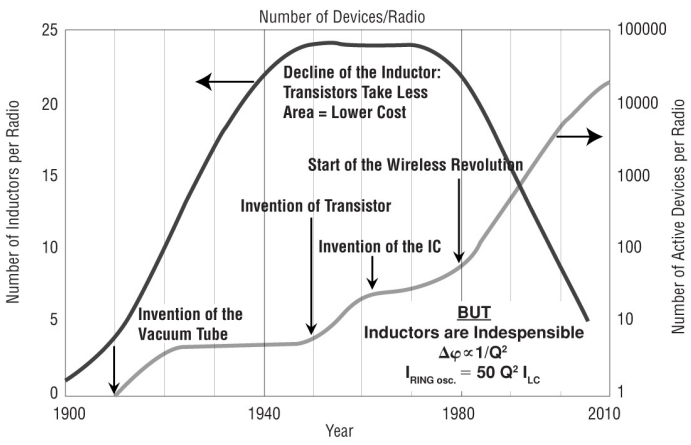


Figure 1.2.13: The rise and fall of the inductor.

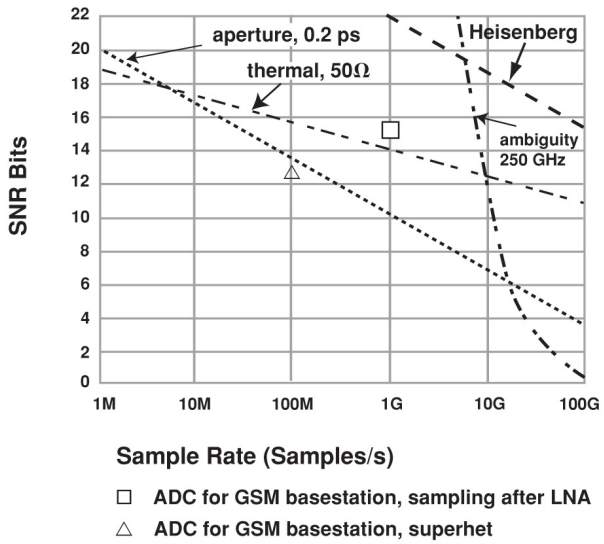


Figure 1.2.14a: Challenges for ADC sample rate and dynamic range.

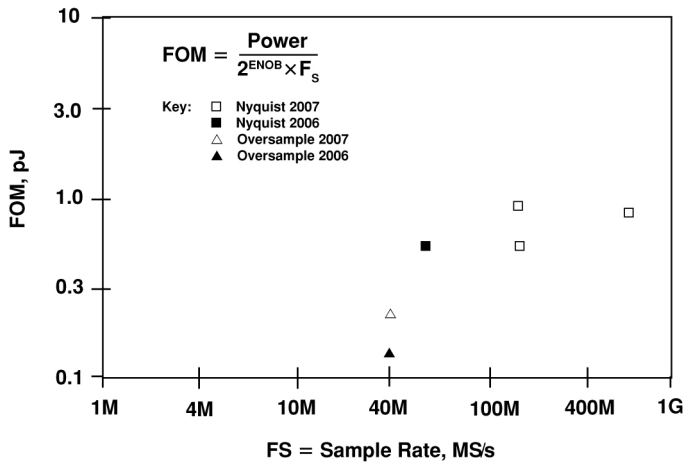


Figure 1.2.14b: Challenges for ADC sample rate and dynamic range.

